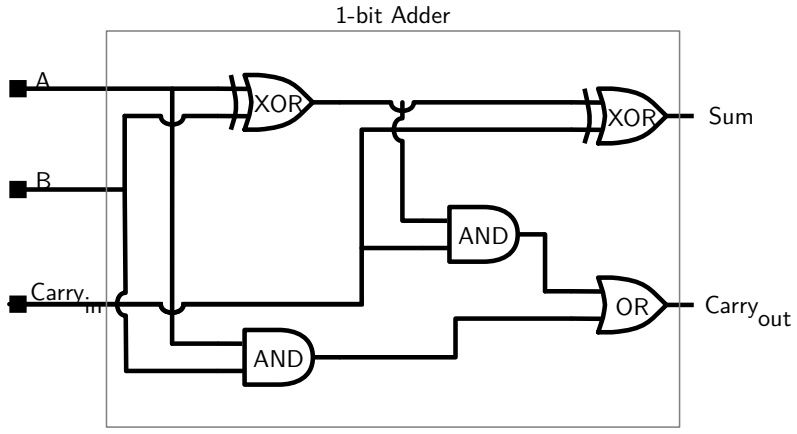

Figure 3.4. Circuit diagram of a "full adder." The inputs are A, B, and C (carry). The outputs is S (the sum) and Cout (carry out). S is true if either A, B, or C are true. If two of them are true then Cout is true and S is false. If all three inputs are true, then both S and Cout are true. Multiple full adders can be chained together to add any number of binary bits.

$$A_3A_2A_1A_0 + B_3B_2B_1B_0 = S_3S_2S_1S_0$$

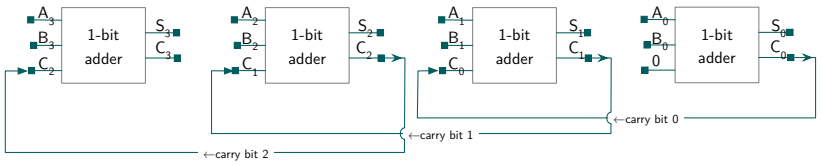

Figure 3.5. Four one-bit full-adders can be combined to form a four-bit adder. Each bit adds the input bits A_n and B_n and the carry bit C_{n-1}. (Note: This four-bit adder ignores the carry bit C_3. As a result, adding `1111` and `0001` will produce `0000`, a condition known as an overflow.) This circuit is "clock-free," meaning that it runs without reference to an external clock, although it may take a few hundred picoseconds for the transistors that make up the gates to stabilize when the logic inputs change. Compare this with Figure 6.3, a 4-bit quantum adder.